WHAT IS CLAIMED IS:

1. A charge-trapping memory cell array comprising:

a semiconductor body;

shallow trench isolations arranged in parallel at a distance to one another at a main surface within said semiconductor body;

memory cells arranged at said main surface of said semiconductor body, each of said memory cells comprising a channel region, first and second source/drain regions formed in said semiconductor body and a memory layer sequence provided for charge-trapping, said channel region being located between said source/drain regions;

wordline stacks arranged in parallel at a distance to one another and running over said channel regions;

bitlines arranged parallel at a distance to one another and running across said wordline stacks; and

local interconnects provided for electric connections between said memory cells and said bitlines, each local interconnect electrically connecting at least two of said source/drain regions and one of said bitlines and comprising an electrically conductive bridge that is arranged above one of said shallow trench isolations such that the local interconnect contacts two of said source/drain regions that are adjacent on both sides of said shallow trench isolation.

2. The charge-trapping memory cell array according to claim 1 wherein the local interconnects are formed of silicon or polysilicon.

3. The charge-trapping memory cell array according to claim 1, wherein:

said memory cells are arranged in a plurality of quadruples, each quadruple comprising a

first memory cell, a second memory cell that is adjacent to said first memory cell in a direction of the wordlines, and a third memory cell and a fourth memory cell that are adjacent to said first and second memory cells, respectively, in a direction of the bitlines;

for a first quadruple, said first source/drain regions of the first, second, third and fourth memory cells are electrically connected by a first one of said local interconnects;

said first memory cell of the first quadruple is also a memory cell of a second quadruple, said second memory cell of the first quadruple is also a memory cell of a third quadruple, said third memory cell of the first quadruple is also a memory cell of a fourth quadruple, and said fourth memory cell of the first quadruple is also a memory cell of a fifth quadruple; and

a second source/drain region of each of said memory cells of the first quadruple is electrically connected to first source/drain regions of a second, third, and fourth memory cell of the respective second, third, fourth or fifth quadruple of memory cells by a second, third, fourth, and fifth one, respectively, of said local interconnects.

4. The charge-trapping memory cell array according to claim 1 wherein said electrically conductive bridges are arranged on the same level as said source/drain regions with respect to said main surface.

5. The charge-trapping memory cell array according to claim 1 wherein said electrically conductive bridges are arranged between lateral boundaries of said source/drain regions that are perpendicular to said main surface.

6. A memory device comprising:

a semiconductor body;

a trench isolation region extending through a portion of the semiconductor body;

a first charge trapping memory cell disposed in the semiconductor body adjacent one edge of the trench isolation region, the first memory cell having a first source/drain region, a second source/drain region and a channel region between the first source/drain region and the second source/drain region;

a second charge trapping memory cell disposed in the semiconductor body adjacent a second edge of the trench isolation region so that the trench isolation region is disposed between the first memory cell and the second memory cell, the second memory cell having a first source/drain region, a second source/drain region and a channel region between the first source/drain region and the second source/drain region; and

a local interconnect region formed over the trench isolation region between the first memory cell and the second memory cell to electrically couple the first source/drain region of the first memory cell to the first source/drain region of the second memory cell, the local interconnect being formed over a recessed portion of the trench isolation region such that the local interconnect abuts a lateral sidewall of the first source/drain region of the first memory cell and also abuts a lateral sidewall of the first source/drain region of the second memory cell.

7. The device of claim 6 wherein the local interconnect region has a top surface that is substantially planar with a top surface of the semiconductor body.

8. The device of claim 6 wherein the local interconnect region comprises silicon or polysilicon.

9. The device of claim 6 wherein the first and second memory cells each include a memory layer sequence provided for charge-trapping.

10. The device of claim 10 wherein the memory layer sequence comprises a first confinement layer, a nitride layer over the first confinement layer, and a second confinement layer over the nitride layer.

11. A method for producing a charge-trapping memory cell array, the method comprising:

providing a semiconductor body having a main surface;

forming a layer sequence on said main surface, the layer sequence including a storage layer;

etching trenches arranged parallel at a distance to one another in said semiconductor body at said main surface;

filling said trenches with a dielectric material to form said shallow trench isolations;

implanting a dopant to form a well of a first conductivity type;

forming wordline stacks running across said shallow trench isolations;

removing upper parts of said shallow trench isolations in said regions provided for local interconnects, thereby forming recesses and exposing lateral surfaces of said semiconductor body in said trenches above remaining lower parts of said shallow trench isolations; and

forming conductive bridges in the recesses of the shallow trench isolations to fill said recesses between said lateral surfaces above said lower parts of said shallow trench isolations.

12. The method of claim 11 and further comprising implanting a dopant for a second electric conductivity type opposite to said first conductivity type, thereby forming source/drain regions and said local interconnects in regions between said wordline stacks and between remaining upper parts of said shallow trench isolations.

13. The method of claim 12 and further comprising forming connecting vias that are electrically insulated from one another and from said wordline stacks to contact said local interconnects from above.

14. The method of claim 11 and further comprising forming oxides on sidewalls of said wordline stacks.

15. The method of claim 11 wherein the wordline stacks are formed by depositing a gate electrode layer, a wordline layer of electrically conductive material, and a hardmask layer and structuring these layers by means of said hardmask layer to form said wordline stacks.

16. The method of claim 11 wherein the conductive bridges are formed from polysilicon or silicon.

17. The method of claim 16 wherein the conductive bridges are formed by selective silicon deposition at said lateral surfaces.

18. The method of claim 11 and further comprising:

filling polysilicon into gaps between said wordline stacks, said polysilicon being made electrically conductive by a dopant;

structuring said polysilicon to form connecting vias; and

filling a dielectric material provided as electric insulation between said connecting vias.

19. The method of claim 11 and further comprising:

filling a dielectric material into gaps between said wordline stacks;

forming contact holes in said dielectric material; and

filling said contact holes with electrically conductive material to form conducting vias.

20. The method of claim 11 wherein the layer sequence includes an oxide layer.

1 21. The method of claim 20 wherein the storage layer comprises a nitride layer.

22. A method for producing a charge-trapping memory cell array, the method comprising:

providing a semiconductor body having a main surface;

forming a layer sequence on said main surface comprising said bottom confinement layer, said storage layer and a preliminary top layer;

etching trenches arranged parallel at a distance to one another in said semiconductor body at said main surface;

filling said trenches with a dielectric material to form said shallow trench isolations;

implanting a dopant to form a well of a first conductivity type;

removing said preliminary top layer at least from areas of said main surface and forming gate oxides, thereby applying said top confinement layer;

depositing a gate electrode layer, a wordline layer of electrically conductive material, and a hardmask layer and structuring these layers by means of said hardmask layer to form said wordline stacks running across said shallow trench isolations;

forming oxides on sidewalls of said wordline stacks;

applying a mask having windows in regions provided for local interconnects;

removing upper parts of said shallow trench isolations in said regions provided for said local interconnects, thereby forming recesses and exposing lateral surfaces of said semiconductor body in said trenches above remaining lower parts of said shallow trench isolations;

forming silicon or polysilicon bridges provided for said local interconnects by selective silicon deposition at said lateral surfaces to fill said recesses between said lateral surfaces above said lower parts of said shallow trench isolations;

removing said mask;

implanting a dopant for a second conductivity type opposite to said first conductivity

type, thereby forming said source/drain regions and said local interconnects in regions between said wordline stacks and between remaining upper parts of said shallow trench isolations; and

forming connecting vias that are electrically insulated from one another and from said wordline stacks to contact said local interconnects from above.

23. The method of claim 22 and further comprising:

filling polysilicon into gaps between said wordline stacks, said polysilicon being made electrically conductive by a dopant;

structuring said polysilicon to form said connecting vias; and

filling a dielectric material provided as electric insulation between said connecting vias.

24. The method of claim 22 and further comprising:

filling a dielectric material into gaps between said wordline stacks;

forming contact holes in said dielectric material; and

filling said contact holes with electrically conductive material to form said conducting vias.

25. The method of claim 22 and further comprising forming said bottom and top confinement layers of oxide.

26. The method of claim 22 and further comprising forming said storage layer of nitride.

27. The method of claim 22 and further comprising:

arranging said local interconnects in such a fashion that in a first quadruple of memory cells comprising a first memory cell, a second memory cell that is adjacent to said first memory

cell in a direction of the wordlines, and a third memory cell and a fourth memory cell that are adjacent to said first and second memory cells, respectively, in a direction of the bitlines, and further comprising a first source/drain region of said first memory cell, a first source/drain region of said second memory cell, a first source/drain region of said third memory cell, and a first source/drain region of said fourth memory cell,

said first source/drain regions are electrically connected by a first one of said local interconnects,

said memory cells of said first quadruple forming first memory cells of a second, third, fourth, and fifth quadruple of memory cells arranged like the first quadruple; and

a second source/drain region of each of said memory cells of the first quadruple is electrically connected to first source/drain regions of a second, third, and fourth memory cell of the respective second, third, fourth or fifth quadruple of memory cells by a second, third, fourth, and fifth one, respectively, of said local interconnects.